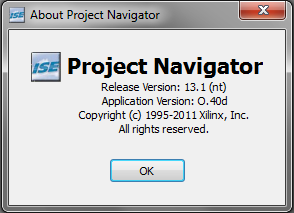
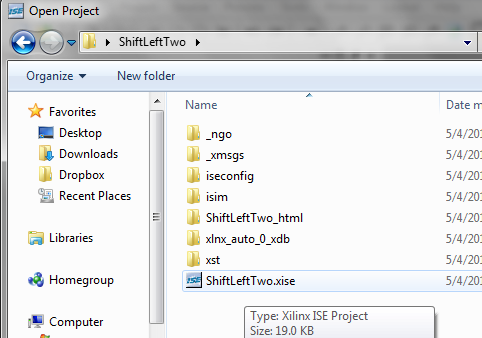
# VIII. Test Procedure

How to create a wave form test case with VHDL Test Bench :

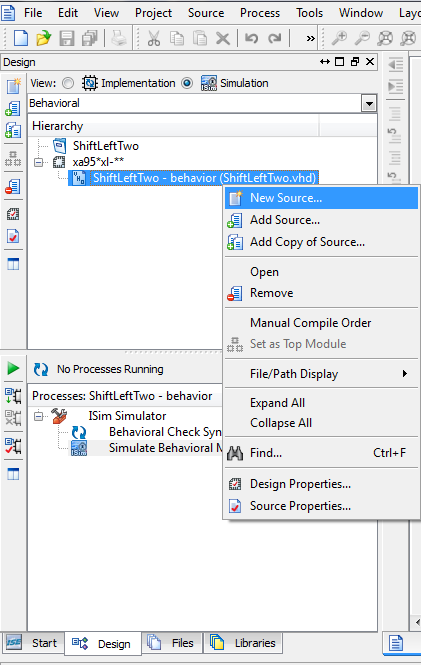
Xilinx Version:



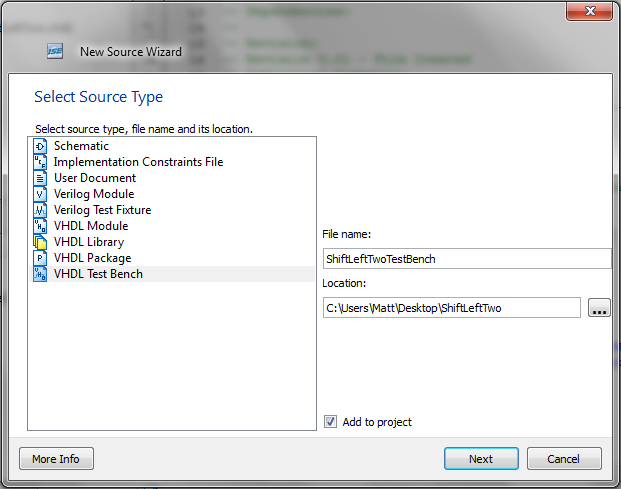
Open an existing Project. For example…



With the *Design* tab selected opened and the Simulation radio button highlighted, right click on the VHDL code Project within the project dropdown and select *New Source…*



Create a new *VHDL Test Bench* and provide it with a useful file name, and click *Next*  twice (one for this screen, and one for the next screen), then finish.



If the project file has been correctly made without any errors, Xilinx will attach the test bench to the selected file that has been mapped to show the current input and output pins. If the file did not automatically generate code for existing inputs and outputs, a possibility is that the file has errors in it and Xilinx WILL NOT attach a test bench to a file that has errors. A test bench not attached to a file will appear as shown below.

The newly generated code has a couple of issues that need to be handled for synchronous devices vs. asynchronous devices.

For SYNCHRONOUS devices, a clock modifier is provided for you as the following:

Clock code:

-- Clock process definitions

clock\_process :process

begin

clock <= '0';

wait for clock\_period/2;

clock <= '1';

wait for clock\_period/2;

end process;

In the ARCHITECTURE of the component, a constant “clock\_period” is set to 10ns. This value can be modified depending on how in depth the outputs from the test bench need to be examined.

For ASYNCHRONOUS devices, the generated clock code described in 5.a can be removed from the test code because no clock is needed to trigger an output for the device. It should look like the following:

-- Clock process definitions

<clock>\_process :process

begin

<clock> <= '0';

wait for <clock>\_period/2;

<clock> <= '1';

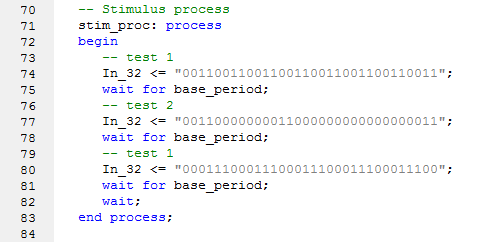
wait for <clock>\_period/2;

end process;

There will still need to be a delay from one test input to the next, however, thus requiring the use of the “<clock>\_period” variable. Just like in step 5.b, rename the variable name to contain only valid characters and set it to 5 ps to start.

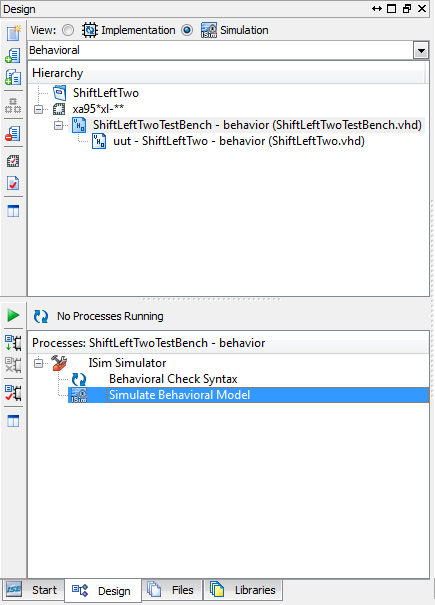
With the clock code squared away, begin to enter in test inputs for the device being tested. This will consist of setting one of the input values to a Boolean character or vector character string.

In our example, we wanted to enter in a 32 bit string into our device, and have it return a value shifted two to the left. We set up the following tests to see if we can achieve that result:



On a side note: removing the wait; at line x82 will continue to run the changes until the test run time finishes.

Once your first round of testing has been attempted, navigate back in the *Design* tab, select *Simulation* radio button at the top and double click on *Simulate Behavioral Model*.



If the file compiled correctly, the simulation will appear in a new window where the last state of the test cases will appear. Depending on the value used as a period in steps 5 or 6, holding the <Control> key while scrolling up and down with the mouse will zoom in and out on the screen.

TROUBLE SHOOTING

Unable to launch application that has no errors:

Be sure that there are no other instances of the Simulator Open

Try Right-Click and selecting *Rerun All* to refresh the system.